CLAIMS

1. A symbol rate processing system for high-speed spread spectrum communications arranged for operation at a specific data rate, comprising programmable hardware blocks running at specific clock frequencies, characterised in that said system comprises programmable registers and comprises means for interleaving, means for error correction and means for rate matching, wherein said clock frequencies are significantly less than the frequencies needed in a DSP-centric approach.

2. The symbol rate processing system as in claim 1, wherein the clock frequencies for the means for interleaving, error correction and rate matching are less than 50 times the data rate.

3. The symbol rate processing system as in claim 1 or 2, wherein the means for error correction comprises one or more elements of the group consisting of a convolutional encoder, a Viterbi decoder, a turbo encoder and a turbo decoder.

4. The symbol rate processing system as in any of the claim 1 to 3, wherein the programmable registers are controlled by a microprocessor subsystem.

5. The symbol rate processing system as in claim 4, wherein the microprocessor subsystem comprises one or more parameters selected from the group consisting of code block length, code rate for error codecs, number of code blocks to be processed, number of fillers to be inserted, numbers of bits to be punctured or repeated, number of iterations in turbo decoding, length of CRC, polynomials for codecs and separate enables/resets for blocks.

6. The symbol rate processing system as in any of the claims 1 to 5, wherein the spread-spectrum communications are selected from the group consisting of

IMT-2000, 3GPP, 3GPP2, W-CDMA, UMTS/FDD, UMTS/TDD, 1xEV-DO, 1xEV-DV, CDMA2000, IS95, IS95A, IS95B, UWB, TD-SCDMA, LAS-CDMA, IEEE802.11, IEEE802.11A, IEEE802.11B or IEEE802.16 communications.

7. An integrated circuit comprising the symbol rate processing system as in any of the claims 1 to 6.

8. A transceiver for high-speed spread spectrum communications comprising the symbol rate processing system as in any of the claims 1 to 6.